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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,314	04/20/2004	Arie Shahar	P-5878-US	2562

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EXAMINER	
BLEVINS, JERRY M	

ART UNIT	PAPER NUMBER
2883	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,314	SHAHAR ET AL.	
	Examiner	Art Unit	
	Jerry Martin Blevins	2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 6, 13, 14, 17, and 19 are objected to because of the following informalities:

In claim 6, the word "fourth" is misspelled as "forth".

In claims 13 and 14, the verb "is" is missing between the words "signal" and "produced".

In claim 17, a comma is needed between the listing of the group of summing gates.

Claim 19 is missing end punctuation.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 7, 9, 15, 16, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent to DiJaili et al., number 6,765,715.

Regarding claim 1, DiJaili teaches an all optical chopping device for shaping and reshaping (Figure 1) comprising an all optical AND logic gate (108, 116 and shown in Figure 10) having a first input (A) for receiving a first optical signal, a second input (B) for receiving a second optical signal and at least one output (X), wherein said AND gate is arranged to produce at said at least one output an optical output signal corresponding to a portion of the AND product of said first optical signal and said second optical signals (column 12, line 26 – column 14, line 4), and wherein said optical output signal is narrower than at least one of said first optical signal and said second optical signal (Figures 2-4).

Regarding claim 2, DiJaili teaches that said first optical signal and said second optical signal are delayed relative to each other (Figures 2-4).

Regarding claim 3, DiJaili teaches that said delay is shorter than one of said first optical signal and said second optical signal (Figures 2-4).

Regarding claim 4, DiJaili teaches that said first optical signal differs from said second optical signal (Figures 2-4).

Regarding claim 7, DiJaili teaches that said first optical signal and said second optical signal arrive from different sources (Figures 1 and 10).

Regarding claim 9, DiJaili teaches that said one of said first input and said second input includes an optical delay line (column 15, line 5 – column 18, line 18).

Regarding claim 15, DiJaili teaches that said optical output signal has the same width as one of said first optical signal and said second optical signal (Figure 2).

Regarding claim 16, DiJaili teaches that said first optical signal and said second optical signal are coherent (column 12, line 26 – column 14, line 4, which teach that the sources are lasers, which produce coherent light).

Regarding claim 18, DiJaili teaches that said AND logic gate includes a threshold device (Figure 1, flop-flop 104).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6, 8, 10-12, 17, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiJaili in view of US Pre Grant Publication to Patel et al., number 2001/0015842.

Regarding claim 5, DiJaili teaches the limitations of the base claim 1. DiJaili does not teach a splitter for receiving and splitting a third optical signal into said first optical signal and said second optical signal. Patel teaches an optical AND gate comprising splitter (Figure 3, beam splitter 88) for receiving and splitting an optical signal into a first optical signal and a second optical signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the splitter of Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Regarding claim 6, DiJaili teaches the limitations of the base claim 1. DiJaili does not teach that said first optical signal and said second optical signal are the split optical components of a fourth optical signal. Patel teaches an optical AND gate wherein a first optical signal and a second optical signal are the split optical components of an optical signal (Figure 3 and page 5, paragraphs 55-57). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the split optical components of Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Regarding claim 8, DiJaili teaches the limitations of the base claim 1. DiJaili does not teach that said first optical signal and said second optical signal arrive from the same source. Patel teaches an optical AND gate wherein a first optical signal and a second optical signal arrive from the same source (Figure 3, source 82). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the first and second optical signals arriving from the same source, as taught by Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Regarding claim 10, DiJaili teaches the limitations of the base claim 1. DiJaili does not teach that said one of said first input and said second input includes an optical amplifier. Patel teaches an optical AND gate wherein one of a first input and a second input includes an optical amplifier (Figure 4, element 132). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the

amplifier of Patel. The motivation would have been to increase the amount of signals which could utilize the AND gate.

Regarding claim 11, DiJaili teaches the limitations of the base claim 1. DiJaili does not teach a closed loop phase control. Patel teaches an optical AND gate comprising a closed loop phase control (Figure 3 and page 5, paragraph 56). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the closed loop phase control of Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Regarding claim 12, DiJaili teaches the limitations of the base claim 1. DiJaili does not teach a closed loop synchronization control. Patel teaches an optical AND gate comprising a closed loop synchronization control (Figure 3 and page 5, paragraph 56). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the closed loop synchronization control of Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Regarding claim 17, DiJaili teaches the limitations of the base claim 1. DiJaili does not teach that said AND logic gate includes a summing gate selected from the group of summing gates containing beam splitters, dielectric beam splitters, metallic beam splitters, dual gratings, interleaved arrayed of waveguides, and dense dual gratings. Patel teaches an AND logic gate including a summing gate containing beam splitters (page 5, paragraph 55). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the beam splitter of Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Regarding claim 19, DiJaili teaches the limitations of the base claim 1. DiJaili does not teach that said AND logic gate includes an optical loop. Patel teaches an AND logic gate including an optical loop (page 5, paragraph 55). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the optical loop of Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Regarding claim 20, DiJaili teaches the limitations of the base claim 1. DiJaili does not teach that said AND logic gate includes a non linear optical loop. Patel teaches an AND logic gate including a non linear optical loop (page 5, paragraph 55). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the non linear optical loop of Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiJaili in view of US Patent to Jensen, number 4,632,518.

Regarding claims 13 and 14, DiJaili teaches the limitations of the base claim 1. DiJaili does not teach that said optical output signal is produced by head or tail chopping of one of said first optical signal and said second optical signal. Jensen teaches an optical AND gate wherein an optical output is produced by chopping an optical signal at an appropriate location, which would include head and tail chopping (column 8, lines 40-56). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the appropriately located chopping of

Jensen. The motivation would have been to improve reliability and accuracy of the phase shifting of the signals (column 8, lines 40-56).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerry Martin Blevins whose telephone number is 571-272-8581. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on 571-272-2415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMB

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